1     151. (Amended) A method of controlling a memory device by a memory
2    controller, wherein the memory device includes a plurality of memory
3    cells, the method of controlling the memory device comprises:
4          providing first block size information to the memory device,
5    wherein the first block size information is provided by the memory
6    controller and [defines] is representative of a first amount of data to
7    be input by the memory device [in response to a write request]; and
8          issuing a first operation code [write request] to the memory
9    device, wherein in response to the first operation code, [write
10   request] the memory device inputs the first amount of data
11   [corresponding to the first block size information].

1     152. The method of claim 151 wherein the memory device inputs the
2    first amount of data synchronously with respect to an external clock
3    signal.

1     153. (Amended) The method of claim 151 further including:
2          providing second block size information to the memory device,
3    wherein the second block size information defines a second amount of
4    data to be input by the memory device [in response to a write request];
5    and
6          issuing a second operation code [write request] to the memory
7    device, wherein in response to the second operation code [write
8    request], the memory device inputs the second amount of data
9    [corresponding to the second block size information].

1     154. (Amended) The method of claim 151 wherein the first block
2    size information and the first operation code [write request] are
3    included in a request packet.

1    155. (Amended) The method of claim 154 wherein the first block
2    size information and the first operation code [write request] are
3    included in the same request packet.

1    156. (Amended) The method of claim 151 further including providing
2    the first amount of data [corresponding to the first block size
3    information] to the memory device.

1    157. The method of claim 156 wherein the first amount of data is
2    provided to the memory device after a delay time transpires.

1    158. (Amended) The method of claim 157 [156] wherein the delay
2    time is representative of a number of clock cycles of [a] an external
3    clock signal.

1    159. (Amended) The method of claim 151 wherein the first block
2    size information is a binary representation of the first amount of data
3    [to be input in response to the first write request].

1    160. (Amended) The method of claim 151 wherein the first amount
2    of data [corresponding to the first block size information] is output,
3    by the memory controller, [input] synchronously during a plurality of
4    clock cycles of an [the] external clock signal.

1    161. (Amended) A method of operation in a synchronous memory
2    device, wherein the memory device includes a plurality of memory cells,
3    the method of operation of the memory device comprises:
4        receiving first block size information from a memory controller,
5    wherein the first block size information [defines] represents a first
6    amount of data to be input by the memory device in response to the
7    operation code [a write request];

8    receiving an operation code, [a first write request] from the

9    memory controller, synchronously with respect to an external clock

10   signal; and

11       inputting the first amount of data [corresponding to the first

12   block size information] in response to the operation code [first write

13   request].


1        162. (Amended) The method of claim 161 wherein inputting the first

2    amount of data includes receiving the first amount of data [the first

3    amount of data corresponding to the first block size information is

4    sampled] synchronously with respect to the external clock signal.


1        163. (Amended) The method of claim 161 wherein the first amount

2    of data is sampled synchronously during a plurality of clock cycles of

3    the external clock signal [further including:

4        [receiving second block size information, wherein the second block

5    size information defines a second amount of data to be input in

6    response to a write request;

7        receiving a second write request from the bus controller; and

8        inputting the second amount of data corresponding to the second

9    block size information], in response to the second operation code write

10   request].


1        164. (Amended) The method of claim 161 wherein the first block

2    size information and the operation code [first write request] are

3    included in a request packet.


1        165. (Amended) The method of claim 164 wherein the first block

2    size information and the operation code [first write request] are

3    included in the same request packet.

1      166. (Amended) The method of claim 161 wherein the first block

2 size information is a binary representation of the first amount of data

3 to be input in response to the <u>operation code</u> [first write

4 request].


1      167. (Amended) The method of claim 161 wherein the first amount

2 of data [corresponding to the first block size information] is [input]

3 <u>output, by the memory controller,</u> synchronously during a plurality of

4 clock cycles of [an] <u>the</u> external clock signal.


1      168. (Amended) The method of claim 161 further including

2 generating an internal clock signal using a delay locked loop and <u>the</u>

3 [an] external clock signal<u>,</u> wherein the first amount of data

4 [corresponding to the first block size information] is input

5 synchronously with respect to the internal clock signal.


1      169. (Amended) The method of claim 161 further including

2 generating first and second internal clock signals using clock

3 generation circuitry and [an] <u>the</u> external clock signal<u>,</u> wherein the

4 first amount of data [corresponding to the first block size

5 information] is input synchronously with respect to the first and

6 second internal clock signals.


1      170. The method of claim 169 wherein the first and second internal

2 clock signals are generated by a delay lock loop.


1      171. (Amended) A method of operation of an integrated circuit,

2 wherein the integrated circuit includes a <u>dynamic random access</u> memory

3 array having a plurality of memory cells, the method of operation

4 comprises:

5      receiving block size information from a controller, wherein the

6 block size information [defines a first] <u>represents an</u> amount of data

7     to be input [from a bus] in response to <u>an operation code</u> [a write
8     request];
9           receiving <u>the operation code from the controller</u> [a first write
10    request]; and
11         inputting the [first] amount of data [corresponding to the block
12    size information] in response to the <u>operation code</u> [first write
13    request].

1         172.  (Amended) The method of claim 171 further including storing
2    the  [first]  amount  of  data  [corresponding  to  the  block  size
3    information]  in  the  memory  array.

1         173.  (Amended) The method of claim 171 wherein the block size
2    information and the <u>operation code</u>  [first write request] are included
3    in  a  request  packet.

1         174.  (Amended) The method of claim 171 wherein the block size
2    information is a binary representation of the [first] amount of data to
3    be  input  in  response  to  the  <u>operation code</u>  [first  write  request].

1         176.  (Amended) The method of claim 171 [161] wherein the [first]
2    amount of data is input, in response to [receipt of] the <u>operation code</u>
3    [first  write  request],  after  a  delay  time  transpires.

1         177.  The  method  of  claim  176  wherein  the  delay  time  is
2    representative of a number of clock cycles of the external clock signal
3    [that  transpire  before  the  first  amount  of  data  is  input].

1         178.  (New) The method of claim 151 wherein the first operation
2    code  is  issued  onto  a  bus.

1      179. (New) The method of claim 178 wherein the bus includes a
2 plurality of signal lines to multiplex control information, address
3 information and data.

1      180. (New) The method of claim 151 further including providing
2 address information to the memory device.

1      181. (New) The method of claim 161 wherein the operation code, the
2 first block size information and address information are included in a
3 packet.

1      182. (New) The method of claim 161 further including receiving
2 address information from the memory controller.

1      183. (New) The method of claim 161 wherein the first block size
2 information, and the operation code are received from an external bus.

1      184. (New) The method of claim 183 wherein the first block size
2 information, and the operation code are received from the same external
3 bus.

1      185. (New) The method of claim 184 wherein the external bus is
2 used to multiplex address information, control information and
3 data.

1      186. (New) The method of claim 171 further including receiving
2 address information from the controller.